What is claimed is:

1. A low dropout voltage regulator (LDO) comprising:

a regulating circuit having an input terminal, an output terminal, and a control terminal, said regulating circuit configured to receive an input signal at said input terminal and provide an output signal at said output terminal in response to a control signal received at said control terminal;

an amplifier having a first and second input terminal and an output terminal, said first input terminal coupled to a first input path, said output terminal of said amplifier coupled to said control terminal of said regulating circuit via a path to provide said control signal; and

a first compensating path coupled between a first node on said first input path and a first node on said path coupling said output terminal of said amplifier to said control terminal of said regulating circuit, said first compensating path comprising a first compensating capacitor.

2. The LDO of claim 1, wherein said first input path comprises a resistor.

3. The LDO of claim 1, further comprising:

a second compensating path coupled between said output terminal of said regulating circuit and a second node on said path coupling said output terminal of said amplifier to said control terminal of said regulating circuit, said second compensating path comprising a second compensating capacitor.

4. The LDO of claim 3, wherein said first input path comprises a resistor.

5. The LDO of claim 4, wherein a feedback network is coupled between said output terminal of said regulating circuit and said second input terminal of said amplifier, wherein a second stage circuit comprises said regulating circuit and said feedback network, and wherein a first dominant pole is introduced in a frequency response plot of said LDO, said first dominant pole given by:

$$f_{p1} = \frac{1}{2\pi\left[R_S(1+A)C_1 + r_{01}(1+B)C_2\right]}$$

where R_S is a value of said resistor, A is a voltage gain of said amplifier, C_1 is a value of said first compensating capacitor, r_{01} is a output impedance of said amplifier, B is a voltage gain of said second stage circuit, and C_2 is a value of said second compensating capacitor.

6. The LDO of claim 4, wherein said first compensating capacitor and said resistor introduce a zero in a frequency response plot of said LDO, said zero given by:

$$f_{z1} = \frac{1}{2\pi R_S C_1}$$

where R_S is a value of said resistor and C_1 is a value of said first compensating capacitor.

7. The LDO of claim 1, wherein said regulating circuit comprises a MOSFET transistor, said input terminal of said regulating circuit comprising a source terminal of said MOSFET transistor, said output terminal of said regulating circuit comprising a drain terminal of said MOSFET transistor, and said control terminal of said regulating circuit comprising a gate terminal of said MOSFET transistor.

8. An integrated circuit comprising:

a load;

at least one low dropout voltage regulator (LDO) for providing a regulated output voltage to said load, said at least one LDO comprising:

a regulating circuit having an input terminal, an output terminal, and a control terminal, said regulating circuit configured to receive an input signal at said input terminal and provide an output signal at said output terminal in response to a control signal received at said control terminal;

an amplifier having a first and second input terminal and an output terminal, said first input terminal coupled to a first input path, said output terminal of said amplifier coupled to said control terminal of said regulating circuit via a path to provide said control signal; and

a first compensating path coupled between a first node on said first input path and a first node on said path coupling said output terminal of said amplifier to said control terminal of said regulating circuit, said first compensating path comprising a first compensating capacitor.

9. The integrated circuit of claim 8, wherein said first input path comprises a resistor.

10. The integrated circuit of claim 8, wherein said at least one LDO further comprises:

a second compensating path coupled between said output terminal of said regulating circuit and a second node on said path coupling said output terminal of said amplifier to said control terminal of said regulating circuit, said second compensating path comprising a second compensating capacitor.

11. The integrated circuit of claim 10, wherein said first input path comprises a resistor.

12. The integrated circuit of claim 11, wherein a feedback network is coupled between said output terminal of said regulating circuit and said second input terminal of said amplifier, wherein a second stage circuit comprises said regulating circuit and said feedback network, and wherein a first dominant pole

is introduced in a frequency response plot of said LDO, said first dominant pole given by:

$$f_{p1} = \frac{1}{2\pi\left[R_S(1+A)C_1 + r_{01}(1+B)C_2\right]}$$

where R_S is a value of said resistor, A is a voltage gain of said amplifier, C_1 is a value of said first compensating capacitor, r_{01} is a output impedance of said amplifier, B is a voltage gain of said second stage circuit, and C_2 is a value of said second compensating capacitor.

13. The integrated circuit of claim 11, wherein said first compensating capacitor and said resistor introduce a zero in a frequency response plot of said LDO, said zero given by:

$$f_{z1} = \frac{1}{2\pi R_S C_1}$$

where R_S is a value of said resistor and C_1 is a value of said first compensating capacitor.

14. An electronic device comprising:

an integrated circuit, said integrated circuit comprising at least one low dropout voltage regulator (LDO), for providing a regulated output voltage to a load of said integrated circuit, said at least one LDO comprising:

a regulating circuit having an input terminal, an output terminal, and a control terminal, said regulating circuit configured to receive an input signal at said input terminal and provide an output signal at said output terminal in response to a control signal received at said control terminal;

an amplifier having a first and second input terminal and an output terminal, said first input terminal coupled to a first input path, said output terminal of said amplifier coupled to said control terminal of said regulating circuit via a path to provide said control signal; and

a first compensating path coupled between a first node on said first input path and a first node on said path coupling said output terminal of said amplifier to said control terminal of said regulating circuit, said first compensating path comprising a first compensating capacitor.

15. The electronic device of claim 14, wherein said first input path comprises a resistor.

16. The electronic device of claim 14, wherein said at least one LDO further comprises:

a second compensating path coupled between said output terminal of said regulating circuit and a second node on said path coupling said output terminal

of said amplifier to said control terminal of said regulating circuit, said second compensating path comprising a second compensating capacitor.

17. The electronic device of claim 16, wherein said first input path comprises a resistor.

18. The electronic device of claim 17, wherein a feedback network is coupled between said output terminal of said regulating circuit and said second input terminal of said amplifier, wherein a second stage circuit comprises said regulating circuit and said feedback network, and wherein a first dominant pole is introduced in a frequency response plot of said LDO, said first dominant pole given by:

$$f_{p1} = \frac{1}{2\pi\left[R_S(1+A)C_1 + r_{01}(1+B)C_2\right]}$$

where R_S is a value of said resistor, A is a voltage gain of said amplifier, C_1 is a value of said first compensating capacitor, r_{01} is a output impedance of said amplifier, B is a voltage gain of said second stage circuit, and C_2 is a value of said second compensating capacitor.

19. The electronic device of claim 17, wherein said first compensating capacitor and said resistor introduce a zero in a frequency response plot of said LDO, said zero given by:

$$f_{z1} = \frac{1}{2\pi R_S C_1}$$

where R_s is a value of said resistor and C_1 is a value of said first compensating capacitor.

20. A method of compensating a low drop out voltage regulator comprising:

introducing a first dominant pole in a frequency response plot of said LDO;

introducing a second parasitic pole in said frequency response plot; and

introducing a first zero in said frequency response plot, said first zero resulting in a first phase shift that at least partially cancels with a second phase shift introduced by said second parasitic pole.

21. The method of claim 20, wherein said second parasitic pole occurs at a first frequency level and said first zero occurs at a second frequency level, said second frequency level less than said first frequency level.